UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,523	10/19/2001	Geetha Pannala	1011-59279	9975

24197 · 7590 03/29/2005	
KLARQUIST SPARKMAN, LLP	EXAMINER
121 SW SALMON STREET	TAT, BINH C
SUITE 1600	
PORTLAND, OR 97204	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/045,523	PANNALA ET AL.
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2004*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some *   c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

U.S. Patent and Trademark Office

PTOL-326 (Rev. 1-04)   Office Action Summary   Part of Paper No./Mail Date 20050317

DETAILED ACTION

1.   This is a response to the response filed on 12/16/04. The applicant argument regarding

Ishikawa et al are not persuasive; therefore, all the rejections based on Ishikawa et al. are

retained and repeated for the following reasons.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claims 1-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al.

(US Patent 6457165).

3.   As to claims 1 (method), 3, 5, 9, 14(machine readable media), 18, 22, 27 (apparatus), 31,

35, Ishikawa et al. teach a computer-implemented method, comprising: inputting a netlist (see

see fig 4 and 9-13); generating symbols and connections formed according to the netlist and at

least in part according to connectivity strength between at least a first symbol and a second

symbol (see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39); and generating a wiring harness

diagram that comprises to the symbols and the connections (see fig 91-13 col 8 lines 56 to col13

lines 64 and col 2 lines 40-57).

4.   As to claims 2 (method), 15(machine readable media), and 28 (apparatus) Ishikawa et al.

teach in which generating the wiring harness diagram comprises: sorting the netlist at least in

part according to the connectivity strength (see col 2 lines 51-57).

5.   As to claims 4 (method), 17(machine readable media), and 30 (apparatus) Ishikawa et al.

teach further comprising: sequencing symbol placement for the wiring harness diagram such that

symbols with predetermined pin positions are placed in the wiring harness diagram with higher

priority than symbols for which the side of the symbol for placing a pin may be selected (see fig

91-13 col 8 lines 56 to col13 lines 64).

6.   As to claims 6 (method), 19(machine readable media), and 32(apparatus) Ishikawa et al.

teach further comprising: selecting a side of a first symbol on which to position a pin to increase

the directness of connectivity between the first symbol and a second symbol (see fig 9-13).

7.   As to claims 7 (method), 20(machine readable media), and 33(apparatus) Ishikawa et al.

teach n which generating a wiring diagram according to the layout further comprises: selecting

sides of the symbols on which to position pins according to a selected layout dimension, and

arranging the pins on the selected sides to increase the directness of connections between the

symbols (see fig 9-13).

8.   As to claims 8 (method), 21(machine readable media), and 34(apparatus) Ishikawa et al.

teach sequencing symbol placement for the wiring harness diagram such that symbols with

predetermined pin positions are placed in the layout with higher priority than symbols for which

the side of the symbol for placing a pin may be selected (see fig 91-13 col 8 lines 56 to col13

lines 64).

9.   As to claims 10(method), 23(machine readable media), and 36(apparatus) Ishikawa et al.

teach in which selecting the side of the first symbol further comprises: selecting the side

according to a selected layout dimension and a position of the second symbol (see fig 91-13 col 8

lines 56 to col13 lines 64).

10.   As to claims 11 (method), 24(machine readable media), and 37 (apparatus) Ishikawa et

al. teach further comprising: sequencing symbol placement for the wiring harness diagram such

that symbols with predefined pin positions are placed in the layout with higher priority than

symbols for which the side of the symbol for placing a pin may be selected (see fig 91-13 col 8

lines 56 to col13 lines 64 and background).

11.   As to claims 12 (method), 25(machine readable media), and 38 (apparatus) Ishikawa et

al. teach A computer-implemented method, comprising: when at least one first pair of symbols of

a netlist has been placed in a wiring harness layout, selecting a next pair of symbols to place in

the layout comprising at least one symbol of the first pair (see fig 9-13 col 8 lines 51-55 and col

2 lines 34-39); and when there is at least one predefined symbol in the netlist, selecting as the

next pair of symbols a pair of symbols having the highest connection strength and comprising a

predefined symbol (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

12.   As to claims 13 (method), 26(machine readable media), and 39 (apparatus) Ishikawa et

al. teach further comprising: selecting for the placement of pins a side of one symbol of the next

pair of symbols (see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39); and arranging the pins

along the side to increase the directness of connection between the next pair of symbols (see fig

9-13 col 8 lines 51-55 and col 2 lines 34-39).

13.   As to claim 16(machine readable media), and 29 (apparatus), Ishikawa et al. teach in

which generating the symbols further comprises: positioning a pin on a side of the first symbol,

the side selected according to (a) a connection between the first symbol and the second symbol

(see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

14.   As to claims 40 Ishikawa et al. teach a carrier wave, comprising: signals defining

component symbols and connections generated according to a netlist and a selected wiring

harness layout dimension, the symbols and connections defining a wiring harness diagram along

the layout dimension (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

15.   As to claims 41 Ishikawa et al. teach A carrier wave, comprising: signals defining a first

and second component symbols, the component symbols comprising pins, the pins positioned on

sides of the symbols selected to increase the directness of connectivity between the first symbol

and the second symbol (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

16.   As to claims 42 Ishikawa et al. teach wherein the wiring harness diagram corresponds to

a wiring harness, the wiring harness comprising at least one bundle of signal-carrying wires (see

fig 9-13 col 8 lines 51-55 and col 2 lines 34-39).

17.   As to claims 43 Ishikawa et al. teach wherein the wiring harness diagram is generated

along a selected wiring harness layout dimension (see fig 9-13 col 8 lines 51-55 and col 2 lines

34-39).

18.   As to claims 44 Ishikawa et al. teach wherein the signal-carrying wires carry electrical

signals (see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39).

19.   As to claims 45 Ishikawa et al. teach wherein the signal-carrying wires carry optical

signals (see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39).

20.   As to claims 46 Ishikawa et al. teach wherein the wiring harness diagram represents a

wiring harness that establishes connectivity between at least two components (see fig 91-13 col 8

lines 56 to col13 lines 64 and background).

21.   As to claims 47 Ishikawa et al. teach wherein at least one component is an electrical

component (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

22.   As to claims 48 Ishikawa et al. teach wherein at least one component is an optical

Component (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

23.   As to claims 49 Ishikawa et al. teach wherein the act of generating a wiring harness

diagram comprises resizing at least one symbol (see fig 91-13 col 8 lines 56 to col13 lines 64 and

background).

24.   As to claims 50 Ishikawa et al. teach wherein the act of generating a wiling harness

diagram comprises repositioning at least one symbol (see fig 91-13 col 8 lines 56 to col13 lines

64 and background).

25.   As to claims 51 Ishikawa et al. teach wherein the wiring harness diagram further

comprises pins, wherein the act of generating the wiring harness diagram comprises arranging

the pins to increase directness of connections between at least two symbols, and wherein at least

one symbol is resized and at least one symbol is repositioned (see fig 91-13 col 8 lines 56 to

col13 lines 64 and background).

26.   As to claims 52 Ishikawa et al. teach wherein arranging the pins comprises resizing at

least one symbol (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

27.   As to claims 53 Ishikawa et al. teach wherein arranging the pins comprises repositioning

at least one symbol (see fig 91-13 col 8 lines 56 to col13 lines 64 and background).

Response to Amendment and Arguments

28.   Applicant's arguments filed September 02, 2004 have been fully considered but they are

not persuasive.

29.   Applicant contends that Ishikawa et al. do not describe "generating symbols and

connections formed according to the netlist and at least in part according to connectivity strength

between at least a first symbol and a second symbol" as claimed. In response to Applicant's

argument that Ishikawa et al. do not describe "generating symbols and connections formed

according to the netlist and at least in part according to connectivity strength between at least a

first symbol and a second symbol" as claimed, Examiner respectfully disagrees. Applicant is

directed to (Ishikawa et al teach the connection routing between two terminal, and generating

wiring harness diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason,

examiner holds the rejection proper.

30.   Applicant contends that Ishikawa et al. do not describe "generating a wiring harness

diagram, wherein the wiring harness diagram comprises the symbols and the connections, and

wherein generating the wiring harness diagram comprises positioning a pin on a side of a first

symbol, the side selected according to a connection between the first symbol and a second

symbol" as claimed. In response to Applicant's argument that Ishikawa et al. do not describe

"generating a wiring harness diagram, wherein the wiring harness diagram comprises the

symbols and the connections, and wherein generating the wiring harness diagram comprises

positioning a pin on a side of a first symbol, the side selected according to a connection between

the first symbol and a second symbol" as claimed, Examiner respectfully disagrees. Applicant is

directed to (Ishikawa et al teach the connection pin (A, B, C, D) routing between two terminal,

and generating wiring harness diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason, examiner holds the rejection proper.

31.   Applicant contends that Ishikawa et al. do not describe "sequencing symbol placement in a wiring harness layout for at least one bundle comprising signal-carriers at least in part according to the connectivity strength of at least one pair of symbols; and selecting a side of a first symbol on which to place a pin to increase the directness of connectivity between the first symbol and a second symbol." as claimed. In response to Applicant's argument that Ishikawa et al. do not describe "sequencing symbol placement in a wiring harness layout for at least one bundle comprising signal-carriers at least in part according to the connectivity strength of at least one pair of symbols; and selecting a side of a first symbol on which to place a pin to increase the directness of connectivity between the first symbol and a second symbol." as claimed, Examiner respectfully disagrees. Applicant is directed to (Ishikawa et al teach the connection pin (A, B, C, D) routing between two terminal, and generating wiring harness diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason, examiner holds the rejection proper.

32.   Applicant contends that Ishikawa et al. do not describe "when at least one first pair of symbols of a netlist has been placed in a wiring harness layout, selecting a next pair of symbols to place in the layout comprising at least one symbol of the first pair; and when there is at least one predefined symbol in the netlist, selecting as the next pair of symbols a pair of symbols having the highest connection strength and comprising a predefined symbol." as claimed. In response to Applicant's argument that Ishikawa et al. do not describe "when at least one first pair of symbols of a netlist has been placed in a wiring harness layout, selecting a next pair of symbols to place in the layout comprising at least one symbol of the first pair; and when there is

at least one predefined symbol in the netlist, selecting as the next pair of symbols a pair of

symbols having the highest connection strength and comprising a predefined symbol." as

claimed, Examiner respectfully disagrees. Applicant is directed to (Ishikawa et al teach the

connection pin (A, B, C, D) routing between two terminal, and generating wiring harness

diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason, examiner holds the

rejection proper.

33.   Applicant contends that Ishikawa et al. do not describe "generating symbols and

connections formed according to the netlist and at least in part according to connectivity strength

between at least a first symbol and a second symbol; and generating a wiring harness diagram

that comprises the symbols and the connections." as claimed. In response to Applicant's

argument that Ishikawa et al. do not describe "generating symbols and connections formed

according to the netlist and at least in part according to connectivity strength between at least a

first symbol and a second symbol; and generating a wiring harness diagram that comprises the

symbols and the connections" as claimed, Examiner respectfully disagrees. Applicant is directed

to (Ishikawa et al teach the connection routing between two terminal, and generating wiring

harness diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason, examiner

holds the rejection proper.

34.   Applicant contends that Ishikawa et al. do not describe "signals defining component

symbols and connections generated according to a netlist and a selected wiring harness layout

dimension, the symbols and connections defining a wiring harness diagram along the layout

dimension." as claimed. In response to Applicant's argument that Ishikawa et al. do not describe

"signals defining component symbols and connections generated according to a netlist and a

selected wiring harness layout dimension, the symbols and connections defining a wiring harness diagram along the layout dimension" as claimed, Examiner respectfully disagrees. Applicant is directed to (Ishikawa et al teach the symbols connection signal routing between two terminal, and generating wiring harness diagram see fig 9-13 col 8 lines 51-55 and col 2 lines 34-39). For this reason, examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art Unit 2825
August 9, 2004

VUTHE SIEK
PRIMARY EXAMINER